

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 57941.000062	SERIAL NUMBER 10716,595
	APPLICANT(S) MICHAEL FARMWALD ET AL.	
	FILING DATE November 20, 2003	GROUP ART UNIT Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNI	1.	4,330,852	May 18, 1982	Redwine et al.	365	221	—
	2.	4,703,418	Oct. 27, 1987	James	700	32	—
	3.	4,726,021	Feb. 16, 1988	Horiguchi et al.	714	723	—
	4.	4,785,394	Nov. 15, 1988	Fischer	700	114	—
TNI	5.	4,870,562	Sept. 26, 1989	Kimoto et al.	711	167	—

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNI	6.	S56-82961	July 7, 1981	Japan	—	—	YES
	7.	S57-14922	Jan. 26, 1982	Japan	—	—	YES
	8.	Sho 60-80193	May 8, 1983	Japan	—	—	YES
	9.	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES
	10.	S61-72350	April 14, 1986	Japan	—	—	YES
	11.	S63-142445	June 14, 1988	Japan	—	—	YES
	12.	B63-46864	Sept. 19, 1988	Japan	—	—	YES
TNI	13.	S64-29951	Jan. 31, 1989	Japan	—	—	YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNI	14.	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
	15.	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
	16.	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
	17.	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
TNI	18.	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER <i>TNI. Nguyen</i>	DATE CONSIDERED <i>03/06/04</i>
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TNI	19.	4,845,670	Jul. 4, 1989	Nishimoto et al.	365	78	—
TNI	20.	4,509,142	Apr. 2, 1985	Childers	711	169	—
TNI	21.	4,685,088	Aug. 4, 1987	Ianucci	365	189,02	—

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNI	22.	0 246 767	April 28, 1987	EPO	—	—	—
TNI	23.	0 334 552	Mar. 16, 1989	EPO	—	—	—
TNI	24.	0 276 871	Jan. 29, 1988	EPO	—	—	—

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNI	25.	European Search Report for EPO Patent Application No. 00 101 1832
	26.	European Search Report for EPO Patent Application No. 89 30 2613
	27.	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
	28.	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
	29.	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
	30.	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
TNI	31.	JEDEC Standard No. 21C

EXAMINER TAN I. NEWTON	DATE CONSIDERED 03/02/04
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TNT	32.	4,649,511	03/10/97	Gdula	711	106	—
	33.	4,860,198	08/22/89	Takenaka	711	127	—
	34.	3,969,706	07/13/76	Proebsting et al.	365	189.02	—
	35.	4,766,536	08/23/88	Wilson, Jr. et al.	710	121	—
	36.	4,998,262	03/05/91	Wiggers	375	376	—
	37.	4,757,473	07/12/88	Kurihara et al.	365	189.12	—
	38.	4,792,926	12/20/88	Roberts	365	189.02	—
	39.	4,811,202	03/07/89	Schabowski	710	127	—
	40.	5,034,917	07/23/91	Bland et al.	711	167	—
	41.	4,845,664	07/04/89	Aichelmann, Jr. et al.	711	405	—
	42.	5,140,688	08/18/92	White et al.	710	600	—
	43.	4,747,079	05/24/88	Yamaguchi	365	189.08	—
	44.	5,301,278	04/05/94	Bowater et al.	711	5	—
	45.	5,051,889	09/24/91	Fung et al.	711	157	—
TNT	46.	5,153,856	10/06/92	Takahashi	365	233	—

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TNT	47.	M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)
TNT	48.	T.L. Jeremiah et. al., "SYNCHRONOUS LSSD PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
TNT	49.	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)

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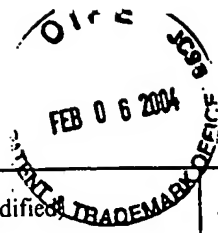
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TNT	50.	04/24/84	Nishiguchi	365	194	—
	51.	04/11/89	Christopher et al.	365	230.03	—
	52.	11/21/89	Ohno et. al.	365	206	—
	53.	08/21/90	Yamaguchi et al.	365	189.02	—
TNT	54.	04/21/92	Fung et al.	365	230.03	—

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TNT	55.	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
	56.	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
	57.	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
	58.	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
	59.	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
	60.	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
	61.	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
	62.	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
	63.	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
	64.	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
	65.	E. H. Frank, "The SBUS: Sun's High Performance Bus for RISC Workstations", Sun Microsystems Inc. 1990
	66.	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
TNT	67.	J. Chun et al. "A pipelined 650MHz GaAs 8K ROM with Translation Logic" GaAs IC Symposium 1990

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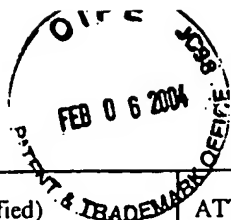


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TNT	68.	5,206,833	04/27/93	Lee	365	233	—
	69.	4,953,128	08/28/90	Kawai et al.	365	194	—
	70.	4,970,418	11/13/90	Masterson	327	141	—
	71.	4,916,670	04/10/90	Suzuki et al.	365	233	—
	72.	4,570,220	02/11/86	Tetrick et al.	710	226	—
	73.	4,099,231	07/01/78	Kotok et al.	711	168	—
	74.	5,301,278	04/05/94	Bowater et al.	711	5	—
	75.	5,140,688	08/18/92	White et al.	710	600	—
	76.	5,018,111	05/21/91	Madland	365	233	—
	77.	4,734,880	03/29/88	Collins	711	105	—
	78.	4,183,095	01/08/80	Ward	365	189.02	—
	79.	4,975,872	12/04/90	Zaiki	365	49	—
	80.	5,016,226	05/14/91	Hiwada et al.	365	233	—
	81.	5,210,715	05/11/93	Houston	365	194	—
	82.	4,928,265	05/22/90	Higuchi et al.	365	189.01	—
	83.	4,953,130	08/28/90	Houston	365	203	—
	84.	5,251,309	10/05/93	Kinoshita et al.	711	167	—
	85.	4,630,193	Dec. 16, 1986	Kris	713	502	—
	86.	4,710,904	Dec. 1, 1987	Suzuki	365	226	—
TNT	87.	4,739,502	Apr. 19, 1988	Nozaki	365	233	—

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TNI	88.	4,205,373	May 27, 1980	Shah et al.	710	128	—
	89.	4,905,201	Feb. 27, 1990	Ohira et al.	365	233.03	—
	90.	3,691,534	09/12/72	Veradi, et. al	365	78	—
	91.	3,771,145	11/06/73	Wiener	365	240	—
	92.	4,536,795	08/20/85	Hirota, et. al	348	774	—
	93.	4,629,909	12/16/86	Cameron	327	211	—
	94.	4,631,659	12/23/86	Hayne, et. al	711	167	—
	95.	4,858,113	08/15/89	Saccardi	710	132	—
	96.	4,499,536	02/12/85	Gemma et al.	711	167	—
TNI	97.	4,648,102	03/03/87	Riso, et. al	375	356	—

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNI	98.	EP 0424774	05/02/91	EPO	—	—	—
TNI	99.	EP 0449052	03/29/90	EPO	—	—	—

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNI	100.	European Search Report for EPO Patent Application No. 00 10 0018
	101.	European Search Report for EPO Patent Application No. 00 10 822
	102.	Takasugi, A. et al., "A Data-Transfer Architecture for Fast Multi-Bit Serial Access Mode DRAM," 11 th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985)
TNI	103.	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)

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TNT	104.	4,663,735	05/05/87	Novak, et. al	345	533	—
	105.	4,825,287	04/25/89	Baji, et. al	348	720	—
	106.	4,845,677	07/04/89	Chappell, et. al	365	189.02	—
	107.	4,873,671	10/10/89	Kowshik, et. al	365	189.12	—
	108.	4,876,670	10/24/89	Nakabayashi, et. al	365	194	—
TNT	109.	4,901,036	02/13/90	Herold, et. al	331	25	—

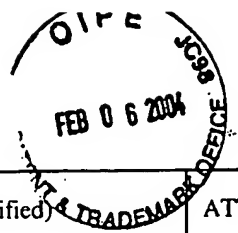
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TNT	110.	EP 0218523	05/30/89	EPO	—	—	
	111.	JP-A-1- 236494	09/21/89	JP	—	—	YES
	112.	Sho 62-71428	03/27/87	JP	—	—	YES
TNT	113.	EP 0282735	09/21/88	EPO	—	—	

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TNT	114.	Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache", IEEE J. Solid State Circuits, vol. SC-22, No. 5, pp. 790-798 (Oct. 1987)
	115.	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)
	116.	1989 GaAs IC Data Book & Designers Guide, Gigabit Logic Inc. (Aug 1989)
	117.	"IC's for Entertainment Electronics, Picture in Picture System Edition 8.89", Siemens AG, 2/89
	118.	Fagan, J.L., "A 16-kbit Nonvolatile Charge Addressed Memory," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5, pp. 631-636 (Oct. 1976)
	119.	Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4Md Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
TNT	120.	Schmitt-Landsiedel, Doris, "Pipeline Architecture for Fast CMOS Buffer RAMs," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)

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TNT	121.	4,979,145	12/18/90	Remington, et. al	711	106	—
	122.	5,099,481	04/24/92	Miller	371	22.1	—
	123.	5,016,226	05/14/91	Hiwada, et. al	365	233	—
	124.	5,023,835	06/11/91	Akimoto, et. al	365	155	—
	125.	5,036,495	07/30/91	Busch, et. al	365	233	—
	126.	5,111,486	05/05/92	Oliboni, et. al	375	376	—
	127.	5,123,100	06/16/92	Hisada, et. al	713	401	—
	128.	5,276,846	01/04/94	Aichelmann Jr., et. al	711	165	—
	129.	5,361,277	11/01/94	Grover	375	356	—
TNT	130.	5,684,753	11/04/97	Hashimoto, et al	365	219	—

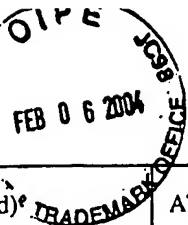
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TNT	131.	WO 89/12936	12/28/89	PCT	—	—	
TNT	132.	JP 62-51509	03/06/87	Japan	—	—	YES

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TNT	133.	Svensson, Christer, "High Speed CMOS Chip to Chip Communications Circuit," IEEE International Symposium on Circuits and Systems, pp. 2228-2231 (Jun. 1991)
	134.	Wakayama, Myles, "A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, pp. 1074-1081 (Dec. 1987)
	135.	Whiteside, Frank, "A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output," IEEE International Solid-State Circuits Conference Digest (Feb. 1986)
	136.	Wu, Jich-Tsormg, "A 100-MHz Pipelined CMOS Comparator," IEEE Journal of Solid-State Circuits, Vol. 23, No. 6, pp. 1379-1385 (Dec. 1988)
TNT	137.	Lineback, J. Robert, "System Snags Shouldn't Slow the Boom in Fast Static RAMs," Electronics, pp. 60-62 (July 23, 1997)

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TNT	138.	Graham, Andy and Stewart Sando, "Pipelined Static RAM Endows Cache Memories with 1-ns Speed," Electronic Design, pp. 157-170 (Dec. 1984)
	139.	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
	140.	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)
	141.	Iqbal, Mohammad Shakaib, "Internally Timed RAMs Build Fast Writable Control Stores," Electronic Design, pp. 93-96 (August 25, 1988)
	142.	Schnaitter, William M. et al., "A 0.5-GHz CMOS Digital RF Memory Chip," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
	143.	Bursky, Dave, "Advanced Self-Timed SRAM Pares Access Time to 5 ns," Electronic Design, pp. 145-147 (Feb. 22, 1990)
	144.	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
	145.	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
	146.	Gregory Uvieghara et al., "An On-Chip Smart Memory for a Data-Flow CPU," IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89 (Feb. 1990)
	147.	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
	148.	Graham, Andy and Stewart Sando, "Pipelined Static RAM Endows Cache Memories with 1-ns Speed," Electronic Design pp. 157-170
	149.	Hans-Jurgen Mattausch et al., "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length," IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988)
TNT	150.	Kanopoulos, Nick and Jill H. Hallenbeck, "A First-In, First-Out Memory for Signal Processing Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)

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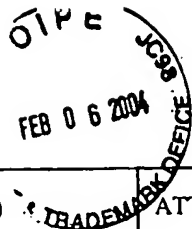
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EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	151.	4,763,249	08/09/88	Bomba et al.	713	600	—
	152.	5,179,667	01/12/1993	Iyer	711	167	—
	153.	5,029,124	07/02/1991	Leahy et al.	710	105	—
	154.	4,878,166	10/31/1989	Johnson et al.	710	127	—
	155.	4,851,990	07/25/1989	Johnson et al.	710	100	—
	156.	4,839,801	06/13/1989	Nicely et al.	710	35	—
	157.	3,950,735	04/13/1976	Patel	710	50	—
	158.	4,933,953	Jun. 12, 1990	Yagi	375	149	—
	159.	5,133,064	Jul. 21, 1992	Hotta et al	709	400	—
	160.	5,184,027	Feb. 2, 1993	Masuda et al.	327	049	—
	161.	4,761,567	Aug. 2, 1988	Walters, Jr. et al.	327	295	—
TNT	162.	5,101,117	Mar. 31, 1992	Johnson et al.	327	149	—

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	163.	SHO 58-192154	Nov. 9, 1983	Japan	—	—	NO
	164.	SHO 63-34795	Feb. 15, 1988	Japan	—	—	NO
	165.	SHO 61-107453	May 26, 1986	Japan	—	—	NO
	166.	SHO 63-91766	April 22, 1988	Japan	—	—	YES
	167.	SHO 62-16289	Jan. 24, 1987	Japan	—	—	NO
	168.	SHO 61-160556	Oct. 4, 1986	Japan	—	—	NO
TNT	169.	JP 1284132	Nov 15, 1989	Japan	—	—	YES

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TNT	170.	4,528,646	Jul. 9, 1985	Ochii et al.	365	203	—
	171.	4,922,141	May 1, 1990	Lofgren et al.	327	244	—
	172.	4,253,147	Feb. 24, 1981	MacDougall et al.	711	169	—
	173.	4,975,877	Dec. 4, 1990	Bell	365	189.01	—
	174.	4,712,194	Dec. 8, 1987	Yamaguchi et al.	365	203	—
TNT	175.	6,345,321	Feb. 5, 2002	Litaize et al.	710	23	—

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	176.	EP 0 329 418 A2	Aug 23, 1989	EPO	—	—	—
	177.	JP 1043894	Feb. 16, 1989	Japan	—	—	YES
	178.	sho 58-31637A	Feb 24, 1983	Japan	—	—	—
	179.	sho 59-165285A	Mar. 11, 1983	Japan	—	—	—
	180.	sho 60-261095A	June 6, 1984	Japan	—	—	—
	181.	sho 63-300310	Dec. 7, 1988	Japan	—	—	—
	182.	hei 2-8950	Jan 12, 1990	Japan	—	—	—
TNT	183.	sho 58-184626A	Oct 28, 1983	Japan	—	—	—

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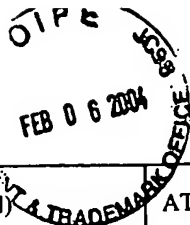
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EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	184.	5,287,532	Feb. 15, 1994	Hunt	712	10	—
	185.	5,157,776	Oct. 20, 1992	Foster	711	131	—
	186.	5,023,838	Jun. 11, 1991	Herbert	365	189.08	—
	187.	4,961,171	Oct. 2, 1990	Pinkham et al.	365	230.05	—
	188.	4,930,065	May 22, 1990	McLagan et al.	710	50	—
	189.	4,641,276	Feb. 3, 1987	Dunki-Jacobs	710	71	—
	190.	4,639,890	Jan. 27, 1987	Heilveil et al.	345	559	—
	191.	4,468,733	Aug. 28, 1984	Oka et al.	710	312	—
	192.	4,426,685	Jan. 17, 1984	Lorentzen	713	401	—
	193.	4,408,272	Oct. 4, 1983	Walters	710	61	—
	194.	4,257,097	Mar. 17, 1981	Moran	711	119	—
	195.	3,846,763	Nov. 5, 1974	Riikonen	710	40	—
TNT	196.	H696	Oct. 3, 1989	Davidson	364	900	—

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	197.	Motorola MC88200 Cache/Memory Management Unit User's Manual, Motorola Inc. 1989
	198.	B. Ramakrishna et al., "The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs" Computer IEEE, Jan 1989 pp. 12-35
	199.	Ralston, E.D. Reilly, "Encyclopedia of Computer Science", Chapman & Hall, 1983, page 1471
TNT	200.	S.A. Ward, R.H. Halstead, "Computation Structures", The MIT Press, McGraw-Hill Book Company, 1990, pages, 174-175, 93, 250-251, and 258-259

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TNT	201.	5,847,997	Dec. 8, 1998	Harada et al.	365	185-33	—
	202.	5,148,523	Sep. 15, 1992	Harlin et al.	345	149	—
	203.	5,142,637	Aug. 25, 1992	Harlin et al.	711	106	—
	204.	5,109,498	Apr. 28, 1992	Kamiya et al.	711	123	—
	205.	4,954,987	Sep. 4, 1990	Auvinen et al.	365	189-02	—
TNT	206.	4,937,734	Jun 26, 1990	Bechtolsheim	711	202	—

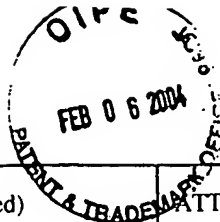
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TNT	207.	61028248	Feb. 7, 1986	Japan	—	—	—

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	208.	Betty Prince, "Semiconductor Memories", Second Edition, John Wiley & Sons, 1991, pages 251, 310, 314, 200-201, 467
	209.	"Intel MCS-4 Micro Computer Set", Intel Corporation, Santa Clara, CA, 1972, (pp.1-12)
	210.	"MIPS R3010 coprocessor", IEEE Micro June 1988, (pp.54-62)
	211.	"Intel MCS-4 Micro Computer Set Users Manual", Intel Corporation, Santa Clara, CA, March 1972, (pp.1-26, and 60-68)
	212.	"Bipolar/MOS Memories Data Book", Advanced Micro Devices, Sunnyvale, CA, 1986 (pp. 4-143 to 4-163)
TNT	213.	"Memories 1986-87 Databook", Fujitsu Inc., 1986 (pp. 1-102 to 1-128)

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TNT	214.	4,920,483	Apr. 24, 1990	Pogue et al.	711	219	—
	215.	4,912,630	Mar. 27, 1990	Cochcroft Jr.	711	211	—
	216.	4,807,189	Feb. 21, 1989	Pinkham et al.	365	189.05	—
	217.	4,799,199	Jan. 17, 1989	Scales, III et al.	365	230.08	—
	218.	4,788,667	Nov. 29, 1988	Nakano et al.	365	193	—
	219.	4,680,738	Jul. 14, 1987	Tam	365	239	—
	220.	4,675,850	Jun. 23, 1987	Kumanoya et al.	365	230.01	—
	221.	4,519,034	May 21, 1985	Smith et al.	710	51	—
	222.	4,315,308	Feb. 9, 1982	Jackson	710	33	—
	223.	4,247,817	Jan. 27, 1981	Heller	327	63	—
	224.	4,092,665	May 30, 1978	Saran	341	63	—
	225.	4,084,154	Apr. 11, 1978	Panigraphi	365	222	—
TNT	226.	3,821,715	Jun. 28, 1974	Hoff, Jr. et al.	711	1	—

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TNT	120553/1987	Jun. 1, 1987	Japan	—	—	—
	0 189 576	Aug. 6, 1986	EPO	—	—	—
	0 187 289	Jul. 16, 1986	EPO	—	—	—
TNT	0 166 192	Jan. 2, 1986	EPO	—	—	—

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TNT	227.	5,598,554	Jan. 28, 1997	Litaize et al.	716	1	—
	228.	4,644,469	Feb. 17, 1987	Sumi	711	211	—
	229.	4,747,081	May 24, 1988	Heilveil et al.	365	219	—
	230.	6,112,287	Aug. 29, 2000	Litaize et al.	712	11	—
TNT	231.	4,782,439	Nov. 1, 1988	Borkar et al.	710	23	—

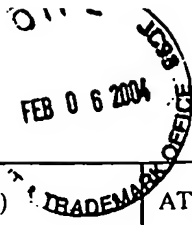
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	232.	0 126 976	Dec. 5, 1984	EPO	—	—	—
	233.	135684/1984	Aug. 3, 1984	Japan	—	—	—
	234.	82/02615	Aug. 5, 1982	PCT	—	—	—
TNT	235.	33471/1982	Feb. 23, 1982	Japan	—	—	—

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	H. J. Mattausch, et al., "A Memory-Based High-Speed Digital Delay Line With a Large Adjustable Length", IEEE Journal of Solid State Circuits, vol. 23, no. 1, Feb. 1988 (pp. 105-110)
	"MIPS Chip Set Implements Full ECL CPU" Microprocessor Report, MicroDesign Resources Inc., Vol. 3: No. 12; Dec. 1989
	"R6000 System Bus & R6020 SBC Specification" MIPS Computer Systems Inc., Sunnyvale, CA, Aug 22, 1989

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	236.	R.A. Volz et al., "POSITION PAPER ON GLOBAL CLOCK FOR THE FUTUREBUS +", SCI - 1989 - doc-59, pp. 1-9
TNT	237.	"ECL bus controller hits 266 Mbytes/s" Microprocessor Report, MicroDesign Resources Inc., Vol. 4: No. 1; Pg. 12, Jan. 24, 1990
	238.	S. Muchmore, "Designing Computer Systems Based on Multibus II", New Electronics, Vol. 20, No. 16, p. 31-32, Aug. 11, 1987.
	239.	"Accordion Start-Stop Sequencer for a Variable Cycle Storage Controller", IBM Technical Disclosure Bulletin, pp. 2074-2075, (a delphion.com reprint on two sheets), Oct. 1986.
	240.	"Motorola 68030 Cache Organization", posting to Internet Newsgroup net.arch by aglew@ccvaxa.UUCP, (a google.com reprint on two sheets), Sep. 29, 1986.
	241.	M. Bazes et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking And Correction", IEEE Journal of Solid State Circuits, Vol. 18, No. 2, pp. 164-172, Apr. 1983.
	242.	R.W. Callahan et al., "Burst-Mode PIO Bus Control", IBM Technical Disclosure Bulletin, Vol. 21, No. 4, pp. 1417-1419, (a delphion.com reprint on two sheets), Sep. 1978.
	243.	Stanley D. Rosenbaum et al., "A 16 384-Bit High-Density CCD Memory", IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, pp. 33-39, Feb. 1976.
	244.	Hopper et al., "Multiple vs. Wide Shared Bus Multiprocessors", Proceedings of the 16 th Annual International Symposium on Computer Architecture, Jerusalem, Israel, June 1989, IEEE Computer Society Press, 1989.
	245.	Geminger et al., "A Survey of Commercial Parallel Processors", Computer Architecture News, Vol. 16, no. 4, Sept. 1988
TNT	246.	Dubois et al., "Effects of Cache Coherency in Multiprocessors", IEEE Transaction in Computers, Vol. C31, No. 11, pgs. 1083-1099, November 1982.

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